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(Not for submission under 37 CFR 1.99)

Application Number	09651924
Filing Date	2000-08-31
First Named Inventor	Michael S. BERTONE
Art Unit	2154
Examiner Name	Dustin Nguyen
Attorney Docket Number	200301853-1

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
DN	1	6546453		2003-04-08	Kessler et al.	
	2	6546465		2003-04-08	Bertone, M. S.	
	3	6567900		2003-05-20	Kessler, R. E.	
	4	6591349		2003-07-08	Steinman et al.	
	5	6622225		2003-09-16	Kessler et al.	
	6	6633960		2003-10-14	Kessler et al.	
	7	6636955		2003-10-21	Kessler et al.	
DN	8	6654858		2003-11-25	Asher et al.	

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DN	9	6662265		2003-12-09	Kessler et al.	
	10	6662319		2003-12-09	Webb, Jr., et al.	
	11	6668335		2003-12-23	Breach et al.	
	12	6671822		2003-12-30	Asher et al.	
	13	6678840		2004-01-13	Kessler et al.	
	14	6681295		2004-01-20	Root et al.	
	15	6704817		2004-03-09	Steinman et al.	
	16	6715057		2004-03-30	Kessler et al.	
	17	6738836		2004-05-18	Kessler et al.	
	18	6751721		2004-06-15	Webb, Jr., et al.	
DN	19	6754739		2004-06-22	Kessler et al.	

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DN	20	6779142		2004-08-17	Bhavsar et al.	
DN	21	6961781		2005-11-01	Mukherjee et al.	
DN	22	7099913		2006-08-29	Bertone et al.	

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DN	i	David H. ASHER et al., "A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System," U.S. Patent Application Serial No. 09/653,092, August 31, 2000 (39 p.), application now abandoned.	<input type="checkbox"/>


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DN	2	Alpha Architecture Reference Manual, Third Edition, The Alpha Architecture Committee, 1998 (month unknown) Digital Equipment Corporation (21 p.), in particular pages 3-1 through 3-15.	<input type="checkbox"/>
	3	A Logic Design Structure For LSI Testability, E. B. Eichelberger et al., 1977 (month unknown) IEEE (Pages 462-468).	<input type="checkbox"/>
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	5	Testability Features of AMD-K6 Microprocessor, R. S. Fetherston et al., Advanced Micro Devices, 1997 (month unknown) (8 p.).	<input type="checkbox"/>
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	7	Cellular Disco: resource management using virtual clusters on shared-memory multiprocessors, K. Govil et al., 1999 (month unknown) ACM 1-58113-140-2/99/0012 (16 p.).	<input type="checkbox"/>
	8	Rambus RIMM Module (with 128/144Mb RDRAMs), Preliminary Information, Document DL0084 Version 1.1, April 2000 (12 p.).	<input type="checkbox"/>
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